WHAT IS CLAIMED IS:

1. A semiconductor package, comprising:

a semiconductor die;

a substrate including a conductive circuit pattern for connecting electrical connections of the semiconductor die to a plurality of bottom-side terminals accessible from the bottom side of the substrate, wherein the semiconductor die is mounted on a top surface of the substrate;

an encapsulation covering the semiconductor die and at least the top surface of the substrate;

a plurality of top-surface terminals disposed on the top surface of the encapsulation for mounting and electrically connecting to a piggybacked semiconductor package, and wherein the top-surface terminals are electrically connected to at least one of the conductive circuit pattern of the substrate, the electrical connections of the semiconductor die and the bottom-side terminals.

2. The semiconductor package of Claim 1, wherein the top-surface terminals are provided by conductor-filled vias provided through the encapsulation and terminating on the conductive pattern of the substrate, whereby an electrical interface of the piggybacked semiconductor package is accessible via connection to the circuit pattern of the substrate.

3. The semiconductor package of Claim 2, wherein the conductive pattern connects the vias to the bottom-side terminals so that an electrical interface of the piggybacked semiconductor package is accessible via connection to the bottom-side terminals.

4. The semiconductor package of Claim 2, wherein the conductive pattern connects the vias to the electrical connections of the semiconductor die so that an electrical interface of the piggybacked semiconductor package is connected to the semiconductor die.

5. The semiconductor package of Claim 1, wherein the top-surface terminals are provided by conductor-filled vias provided through the encapsulation and terminating on electrical connections of the semiconductor die provided on the top surface of the semiconductor die, whereby an electrical interface of the piggybacked semiconductor package is connected to the semiconductor die.

6. The semiconductor package of Claim 1, wherein the top-surface terminals are provided by conductor-filled vias provided through the encapsulation and substrate terminating and are accessible from the bottom side of the substrate, and wherein at least one of the bottom-side terminals is provided by a bottom side of one of the vias, whereby an electrical interface of the piggybacked semiconductor package accessible from the bottom side of the semiconductor package.

7. The semiconductor package of Claim 1, wherein the top-surface terminals form a grid array land configuration for mounting and electrically connecting a grid array semiconductor package as the piggyback semiconductor package.

8. The semiconductor package of Claim 1, wherein the top-surface terminals are formed by plated vias extending through the encapsulation to at least one of the conductive circuit pattern of the substrate, the electrical connections of the semiconductor die and the bottom-side terminals, and wherein the vias have a conical cross section, whereby plating uniformity is improved.

9. The semiconductor package of Claim 1, wherein the top-surface terminals are formed by vias filled with conductive paste and extending through the encapsulation to provide an interconnect to at least one of the conductive circuit pattern of the substrate, the electrical connections of the semiconductor die and the bottom-side terminals.

10. An electronic assembly, comprising:

a first semiconductor package including an encapsulation housing a semiconductor die and having a first plurality of terminals disposed on a top surface and a second plurality of terminals disposed on a bottom side thereof;

a second semiconductor package having a third plurality of terminals connected to the first plurality of terminals whereby the second semiconductor package is mechanically mounted to the first semiconductor package; and

a printed circuit board having a plurality of lands connected to the second plurality of terminals of the first semiconductor package whereby the first semiconductor package is electrically connected to circuit patterns on the printed circuit board.

11. The electronic assembly of Claim 10, wherein the first plurality of terminals is provided by a top surface of a plurality of vias extending through the encapsulation of the first semiconductor package.

12. The electronic assembly of Claim 10, wherein the second semiconductor package is a flip-chip package and further comprising a plurality of solder balls bonded between terminals on a bottom side of the flip-chip package and the first plurality of terminals of the first semiconductor package.

13. The electronic assembly of Claim 10, wherein the second semiconductor package is a flip-chip package having a plurality of posts on a bottom side thereof forming said third plurality of terminals, and wherein said plurality of posts is bonded to the first plurality of terminals of the first semiconductor package.

14. The electronic assembly of Claim 10, wherein the second semiconductor package is a ball grid array package and wherein the third plurality of terminals comprises a plurality of solder balls and wherein the solder balls are bonded to the first plurality of terminals of the first semiconductor package.

15. The electronic assembly of Claim 10, wherein the second semiconductor package is a land grid array package and wherein the third plurality of terminals comprises a plurality of lands paste-bonded to the first plurality of terminals of the first semiconductor package.

16. A method of manufacturing a semiconductor package, comprising:

mounting a semiconductor die to a substrate;

electrically connecting the semiconductor die to a circuit pattern of the substrate, wherein the substrate has a plurality of bottom side electrical terminals on a bottom side for providing electrical connection to the semiconductor die;

encapsulating the semiconductor die and at least the top surface of the substrate to form an encapsulation;

ablating via holes through the encapsulation; and

depositing conductive material within the via holes to form a plurality of top-surface terminals on the top surface of the semiconductor package for connecting a piggyback semiconductor package to the semiconductor package.

17. The method of Claim 16, wherein the ablating is performed by a laser.

18. The method of Claim 16, wherein the ablating ablates the encapsulant to expose a circuit pattern on the top surface of the substrate, and wherein the depositing generates a via that provides electrical connection from at least one of the plurality of top-surface terminals to the circuit pattern.

19. The method of Claim 16, wherein the ablating ablates the encapsulant to expose an electrical connection on a top surface of the semiconductor die, and wherein the depositing generates a via that provides electrical connection from at least one of the plurality of top-surface terminals to the electrical connection of the semiconductor die.

20. The method of Claim 16, wherein the ablating ablates the encapsulant and the substrate, and wherein the depositing generates a via that provides electrical connection from at least one of the plurality of top-surface terminals to a corresponding on of the plurality of bottom side terminals.